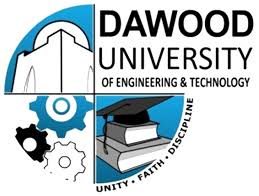
**DIGITAL LOGIC DESIGN**

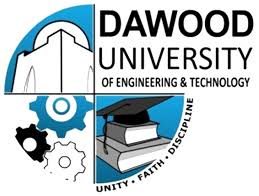
**LABORATORY MANUAL**

**SEMESTER III**

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**DEPARTMENT OF COMPUTER SYSTEM ENGINEERING**

**DAWOOD UNIVERSITY OF ENGINEERING AND TECHNOLOGY KARACHI**

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**DEPARTMENT OF COMPUTER SYSTEM ENGINEERING**

**DIGITAL LOGIC DESIGN**

**LABORATORY MANUAL**

**Course Team**

Engr . Shamim-ur-Rehman Naich

Engr. Abdul Manan Memon

**January 2019**

**PURPOSE**

To help the students to experiment on digital logic design using kits.

**INSTRUCTIONAL OBJECTIVES**

To carry out experiments on various digital logic systems using kits.

**LIST OF EXPERIMENTS**

1. Kl-300 Digital Trainer
2. Basic Logic Gates (And, Or & Not)
3. DE Morgan’s Theorem
4. Nand, Nor, Exclusive Or (Ex-Or), Exclusive Nor (Ex-Nor) Gates
5. Binary Half Adder & Binary Full Adder
6. Binary Half Subtractor & Binary Full Subtractor
7. 7 Segment Display
8. 555 Timer IC
9. Digital Comparator
10. Parity Generator and Checker
11. BCD To Excess -3 Code Converter
12. Multiplexer and Demultiplexer
13. Encoder and Decoder
14. Shift Registers
15. FlipFlop
16. Project

**DAWOOD UNIVERSITY OF ENGINEERING AND TECHNOLOGY KARACHI**

**DEPARTMENT OF COMPUTER SYSTEM ENGINEERING**

Sub Code: Semester: III

Sub Title: Digital Logic Design Course Time: Jul–Nov 2018

Prerequisite: Basic Electronics

**COURSE LEARNING OUTCOME (CLO)**

After the successful completion of course, the students will be able to:

**CLO-1**: Identify and explain fundamental concepts of digital logic design including basic and universal gates, number systems, and Binary coded systems, Basic components of combinational and sequential circuits.

**CLO-2**: Demonstrate the acquired knowledge to apply techniques related to the design and analysis of digital electronic circuits including Boolean algebra and multi-variable Karnaugh map methods.

**CLO-3**: Analyse small-scale combinational and sequential digital circuits.

**CLO-4**: To develop communication skills & team work through group discussion, analysis & investigation, case study, research and presentation of course recent applications.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **ASSESSMENT ACTIVITIES**: | | | | |
| **No.** | **Assessment Activities** | **Marks out of 50** | **Total activities** | **CO Number** |
| 01 | Lab Manual | 10 | 15 | 1-4 |
| 02 | Project Submission | 10 | 01 | 4 |
| 03 | Final Lab Exam | 15 | 01 | 1-4 |
| 04 | Final Viva | 15 | 01 | 1-4 |

**Mapping of Course Outcomes to Program Outcomes**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PO NO.** | **PROGRAM OUTCOMES** | **CONTRIBUTION** | **CLO NO.** | **COMMENTS** |
| **PO-1** | **Engineering Knowledge** | **100%** | **CLO-1** |  |
| **PO-2** | **Problem Analysis** | **100%** | **CLO-3** |  |
| **PO-3** | **Design Development of Solutions** | **50%** | **CLO-2** |  |
| **PO-4** | **Investigations** |  |  |  |
| **PO-5** | **Modern Tool usage** | **50%** | **CLO-2** |  |
| **PO-6** | **The Engineer & Society** |  |  |  |
| **PO-7** | **Environment & Sustainability** |  |  |  |
| **PO-8** | **Ethics** |  |  |  |
| **PO-9** | **Individual & Team Work** | **30%** | **CLO-4** |  |
| **PO-10** | **Communication** | **30%** | **CLO-4** |  |
| **PO-11** | **Project Management** | **40%** | **CLO-4** |  |
| **PO-12** | **Life Long Learning** |  |  |  |

**DAWOOD UNIVERSITY OF ENGINEERING AND TECHNOLOGY KARACHI**

**DEPARTMENT OF COMPUTER SYSTEM ENGINEERING**

Sub Code: Semester: III

Sub Title: Digital Logic Design Course Time: Jul–Nov 2018

Prerequisite: Basic Electronics

**COURSE LEARNING OUTCOME (CLO)**

**CLO-1**: **Student will be able to Identify and explain fundamental concepts of digital logic design including basic and universal gates, number systems, and Binary coded systems, Basic components of combinational and sequential circuits.**

**Experiment 1:** Familiarization with the use of Digital Trainer KL-300 Digital Logic Lab. **[PO-1]**

**Experiment 2:** To study the truth tables of various basic logic gates & to introduce the TTL integrated circuit AND, OR and NOT (inverter) gates. **[PO-1]**

**Experiment 3:** Verification and Interpretation of Truth Tables for Nand, Nor, Exclusive Or (Ex-Or), Exclusive Nor (Ex-Nor) Gates. **[PO-1]**

**Experiment 4:** Illustration of DE Morgan’s Theorem & to Realize Sum of Product (SOP) And Product of Sum (POS) Expressions Using Universal Gates. **[PO-1]**

**CLO-2: Student will be able to demonstrate the acquired knowledge to apply techniques related to the design and analysis of digital electronic circuits including Boolean algebra and multi-variable Karnaugh map methods.**

**Experiment 5:** To Design and Set up a Half Adder & Full Adder Using XOR Gates and NAND Gates. **[PO-3]**

**Experiment 6:** To Identify the Half-Subtractor & Full-Subtractor Circuit Using Logic Gates and Demonstrate Its Operation. **[PO-3]**

**Experiment 7:** To Design and Setup Single Bit Comparator Using Logic Gates and Verify the Truth Table. **[PO-3, PO-2]**

**CLO-3: Analyse small-scale combinational and sequential digital circuits.**

**Experiment 8:** To Design and Verify the Truth Table of A Three Bit Odd Parity Generator And

Checker. **[PO-2, PO-3, PO-5]**

**Experiment 9:** To Design and Set Up the Circuit of BCD to Excess-3 Converter. **[PO-2, PO-3, PO-5]**

**Experiment 10:** To Design Multiplexer and De Multiplexer and Verify Their Truth Tables. **[PO-2, PO-3, PO-5]**

**Experiment 11:** To Set Up and Verify the Performance of Shift Registers. **[PO-2, PO-3, PO-5]**

**Experiment 12:** To Investigate the Operation of A 7-Segment Display. **[PO-2, PO-3, PO-5]**

**Experiment 13:** To Design and Study the Following Circuits Using 555 Timer. **[PO-2, PO-3, PO-5]**

**LABORATORY POLICIES AND REPORT FORMAT**

Reports are due at the beginning of the lab period. The reports are intended to be a complete documentation of the work done in preparation for and during the lab. The report should be complete so that someone else familiar with digital communication could use it to verify your work. The prelab and post lab report format is as follows:

1. A neat thorough prelab must be presented to your Staff Incharge at the beginning of your scheduled lab period. Lab reports should be submitted on A4 paper. Your report is a professional presentation of your work in the lab. Neatness, organization, and completeness will be rewarded. Points will be deducted for any part that is not clear.

2. In this laboratory students will work in teams of three. However, the lab reports will be written individually. Please use the following format for your lab reports.

a. Cover Page: Include your name, Subject Code, Section No., Experiment No. and Date.

b. Objectives: Enumerate 3 or 4 of the topics that you think the lab will teach you. DO NOT REPEAT the wording in the lab manual procedures. There should be one or two sentences per objective. Remember, you should write about what you will learn, not what you will do.

c. Questions: Specific questions (Prelab and Post lab) asked in the lab should be answered here. 3. Your work must be original and prepared independently. However, if you need any guidance or have any questions or problems, please do not hesitate to approach your staff incharge during office hours. Copying any prelab/postlab will result in a grade of 0. The incident will be formally reported to the University and the students should follow the dress code in the Lab session.

4. Each laboratory exercise (circuit) must be completed and demonstrated to your Staff Incharge in order to receive working circuit credit. This is the procedure to follow: a. Circuit works: If the circuit works during the lab period (3 hours), call your staff incharge, and he/she will sign and date it.. This is the end of this lab, and you will get a complete grade for this portion of the lab. b. Circuit does not work: If the circuit does not work, you must make use of the open times for the lab room to complete your circuit. When your circuit is ready, contact your staff incharge to set up a time when the two of you can meet to check your circuit.

5. Attendance at your regularly scheduled lab period is required. An unexpected absence will result in loss of credit for your lab. If for valid reason a student misses a lab, or makes a reasonable request in advance of the class meeting, it is permissible for the student to do the lab in a different section later in the week if approved by the staff incharge of both the sections. Habitually late students (i.e., students late more than 15 minutes more than once) will receive 10-point reductions in their grades for each occurrence following the first.

6. Final grade in this course will be based on laboratory assignments. All labs have an equal weight in the final grade. Grading will be based on pre-lab work, laboratory reports, post-lab and in-lab performance (i.e., completing lab, answering laboratory related questions, etc.,).The Staff Incharge will ask pertinent questions to individual members of a team at random. Labs will be graded as per the following grading policy: Pre-Lab Work 10.00% In-Lab Performance 20.00% Post Lab Work 10.00%

7. Reports Due Dates: Reports are due one week after completion of the corresponding lab. A late lab report will have 10% of the points deducted for being one day late. If a report is 2 days late, a grade of zero will be assigned.

8. Systems of Tests: Regular laboratory class work over the full semester will carry a weightage of 75%. The remaining 25% weightage will be given by conducting an end semester practical examination for every individual student.

**DAWOOD UNIVERSITY OF ENGINEERING AND TECHNOLOGY KARACHI**

**DEPARTMENT OF COMPUTER SYSTEM ENGINEERING**

Sub Code: Semester: III

Sub Title: **Digital Logic Design** Course Time: **Jul–Nov 2018**

**Name :**

**ID No. :**

**Venue :** Digital Electronics Lab

**Lab No. :**

**Title of Experiment:**

**Date of Conduction:**

**Date of Submission:**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max.**  **Marks** | **Marks**  **Obtained** |
| **Lab Performance** |  |  |
| **Lab Report** |  |  |
| **Project** |  |  |
| **Total** | **50** |  |

**REPORT VERIFICATION**

**Date :**

**Teacher Name : Engr. Abdul Manan Memon.**

**Signature :**